

WHAT IS CLAIMED IS:

1 1. A matrix switch circuit, comprising:
2 total $(n \times m)$ pieces of m-to-1 selectors to which one frame
3 where n (n: positive integer) pieces of unit data are serially
4 arrayed is input by m (m: positive integer) pieces in parallel,
5 from which predetermined one frame specified in an address is
6 output and which are divided into m pieces of groups each of
7 which includes n pieces;

8 $(n \times m)$ pieces of selecting circuits that respectively
9 receive the output of the m-to-1 selector and respectively select
10 specific unit data specified in an address in one frame;

11 m pieces of n-to-1 selectors that respectively receive
12 data output from n pieces of selecting circuits, respectively
13 forms and outputs one frame; and

14 a control circuit that sends a control signal to the
15 selecting circuits and the n-to-1 selectors.

1 2. A matrix switch circuit, comprising:

2 total $(n \times m)$ pieces of m-to-1 selectors to which one frame
3 where n (n: positive integer) pieces of unit data are serially
4 arrayed is input by m (m: positive integer) pieces in parallel,
5 from which predetermined one frame specified in an address is
6 output and which are divided into m pieces of groups each of
7 which includes n pieces;

8 $(n \times m)$ pieces of selecting circuits that respectively
9 receive the output of the m-to-1 selector and respectively
10 selects specific unit data specified in an address in one frame;

11 m pieces of n-to-1 selectors that respectively receive
12 data output from n pieces of selecting circuits, respectively
13 forms and outputs one frame; and
14 a control circuit that sends a control signal to the
15 selecting circuits and the n-to-1 selectors, wherein:
16 data input to the matrix switch circuit is p (p: positive
17 integer)-bit parallel data; and
18 (p x n x m) pieces of m-to-1 selectors are arranged, (p
19 x m) pieces of n-to-1 selectors are arranged and (p x m) pieces
20 of input/output lines are arranged.

1 3. A matrix switch circuit according to Claim 1,
2 wherein:

3 data input to the matrix switch circuit is p (p: positive
4 integer)-bit serial data.

1 4. A matrix switch circuit according to Claim 1,
2 wherein:

3 the selecting circuit is provided with first and second
4 circuits to which data output from the m-to-1 selector is written
5 and from which the written data is read and a switching circuit
6 that switches these circuits.

1 5. A matrix switch circuit according to Claim 4,
2 wherein:

3 the first and second circuits are a flip-flop circuit.

1 6. A matrix switch circuit according to Claim 4,

2 wherein:

3 the first and second circuits are arranged in parallel
4 with the m-to-1 selector.

1 7. A matrix switch circuit according to Claim 4,

2 wherein:

3 the first and second circuits are cascaded for the m-to-1
4 selector.

1 8. A matrix switch circuit according to Claim 7,

2 wherein:

3 the first circuit on the side of the m-to-1 selector is
4 a reset-set flip-flop circuit.

1 9. A matrix switch circuit according to Claim 1,

2 wherein:

3 the unit data is a synchronous transfer signal (STS)-1.

1 10. A matrix switch circuit according to Claim 2,

2 wherein:

3 the unit data is a synchronous transfer signal (STS)-1.

1 11. A matrix switch circuit according to Claim 1,

2 wherein:

3 the m-to-1 selector comprises:

4 m pieces of 2-input AND gates;

5 one m-input OR gate connected to the m pieces of 2-input
6 AND gates; and

7 a decoder to which address information is input, wherein:
8 a data input line and an output line of the decoder are
9 connected to each 2-input AND gate; and
10 the m-input OR gate outputs the output of predetermined
11 one 2-input AND gate.

1 12. A matrix switch circuit according to Claim 11,
2 wherein:

3 data input to the m-to-1 selector is p (p: positive
4 integer)-bit parallel data;
5 (p x m) pieces of 2-input AND gates are arranged; and
6 p pieces of m-input OR gates are arranged.

1 13. A matrix switch circuit according to Claim 1,
2 wherein:

3 the m-to-1 selector comprises:
4 m pieces of 2-input AND gates;
5 q ($q < m$) pieces of AND gates;
6 q pieces of selectors; and
7 a q-input OR gate, wherein:
8 the m pieces of 2-input AND gates are divided into q pieces
9 of groups;
10 a data input line and an output line of the AND gate are
11 connected to each 2-input AND gate;
12 the output of the 2-input AND gate in each group is input
13 to one selector;
14 the output of q pieces of selectors is input to the OR
15 gate; and

16 address information is input to the q pieces of AND gates
17 and the q pieces of selectors.

1 14. A matrix switch circuit according to Claim 13,
2 wherein:

3 data input/output to/from the m-to-1 selector is p (p:
4 positive integer)-bit parallel data;
5 (p x m) pieces of 2-input AND gates are arranged;
6 (p x q) pieces of AND gates are arranged;
7 (p x q) pieces of selectors are arranged; and
8 p pieces of q-input OR gates are arranged.

1 15. A matrix switch circuit according to Claim 1,
2 wherein:

3 at least one m-to-1 selector is formed by a field
4 programmable gate array.

1 16. A matrix switch circuit according to Claim 2,
2 wherein:

3 at least one m-to-1 selector is formed by a field
4 programmable gate array.

1 17. A matrix switch circuit according to Claim 1,
2 comprising:

3 a 2-input AND gate that sends a signal to each m-to-1
4 selector, wherein:

5 unit data is input to one input terminal of the 2-input
6 AND gate and a signal output from the selecting circuit is input

7 to the other terminal.

1 18. A matrix switch circuit according to Claim 1,

2 comprising:

3 a 2-input AND gate that sends a signal to each m-to-1
4 selector, wherein:

unit data is input to one input terminal of the 2-input AND gate and the output of a decoder circuit that decodes and outputs address information is input to the other terminal.